Claims

What is claimed as new and desired to be protected by Letter Patent of the United States is:

1. A demodulator for phase modulated (PM) signals comprising:
   A direct phase sampler / digitizer;
   A differencing circuit;
   A "p" deep running averager;
   A digital subtractor;
   A phase to amplitude converter.
2. A demodulator as in claim 1, wherein the direct phase digitizer provides the instantaneous phase of the input signal, at the time of the clock transitions.
3. A demodulator as in claim 1, wherein a differencing circuit generates on every clock cycle the phase difference in the input signal over the clock period.
4. A demodulator as in claim 1, wherein a running averager generates a running average of phase differences over the last "p" consecutive phase differences.
5. A demodulator as in claim 1, wherein a subtractor subtracts the average phase difference generated by the averager from the instantaneous phase difference calculated by the differencing circuit and generates a digital data which indicates the instantaneous phase deviation.
6. A demodulator as in claim 1, wherein a phase to amplitude converter converts the instantaneous phase deviation generated by the subtractor into an amplitude directly proportional to the phase deviation.
7. A running averager as in claim 4, wherein "p" the depth of the averaging span determines the precision for the center frequency.
8. A phase to amplitude converter as in claim 6, wherein the conversion of phase information into a voltage output is obtained by a sine lookup table followed by a digital to analog converter.
9. A phase to amplitude converter as in claim 6, wherein the conversion of phase information into a voltage output is obtained by converting binary code presentation of the phase information into a Grey code followed by further processing using EXOR functions, bit drivers and a resistive network.
10. A demodulator for frequency modulated (FM) signals comprising:
    A direct phase sampler / digitizer;
    A differencing circuit;
    A "p" deep running averager;
    A second "q" deep running averager

A digital subtractor;

A phase to amplitude converter.

11. A demodulator as in claim 10, wherein the direct phase digitizer provides the instantaneous phase of the input signal, at the time of the clock transitions.
12. A demodulator as in claim 10, wherein a differencing circuit generates on every clock cycle the phase difference in the input signal over the clock period.
13. A demodulator as in claim 10, wherein a running averager generates a running average of phase differences over the last "p" consecutive phase differences.
14. A demodulator as in claim 10, wherein a second running averager generates a running average of phase differences over the last "q" consecutive phase differences.
15. A demodulator as in claim 10, wherein a subtractor subtracts the average phase difference generated by the averager from the instantaneous phase difference calculated by the differencing circuit and generates a digital data which indicates the instantaneous phase deviation.
16. A demodulator as in claim 10, wherein a phase to amplitude converter converts the instantaneous phase deviation generated by the subtractor into an amplitude directly proportional to the phase deviation.
17. A running averager as in claim 13, wherein "p" the depth of the averaging span determines the precision for the center frequency.
18. A second running averager as in claim 14, wherein "q" the depth of the averaging span of the second averager determines the bandwidth of the demodulated signal output.
19. A phase to amplitude converter as in claim 16, wherein the conversion of phase information into a voltage output is obtained by a sine lookup table followed by a digital to analog converter.
20. A phase to amplitude converter as in claim 6, wherein the conversion of phase information into a voltage output is obtained by converting binary code presentation of the phase information into a Grey code followed by further processing using EXOR functions, bit drivers and a resistive network.
21. An FM or PM receiver comprising:

    A quadrature input signal generator;

    A direct digital phase digitizer;

    A digital demodulator.
22. A receiver as in claim 21, wherein the quadrature generation may be obtained by quadrature down conversion or by any type of quadrature power splitter.
23. A demodulator as in claim 21, wherein the direct phase digitizer provides the instantaneous phase of the input signal, at the time of the clock transitions.

24. A receiver as is claim 21, wherein the demodulator contains no tuned or resonant circuits and wherein the operation of the demodulator is controlled by a clock.
25. A converter to convert binary code presentation of the phase of a signal into a magnitude of voltage or current comprising:
    EXOR Logic to convert the binary code into Grey code;
    EXOR logic to generate specific driver code;
    A resistive network to convert the drive code into a voltage or current.
26. A converter as in claim 25, wherein the conversion of binary code to Grey code is obtained using the formula $G_n = B_n \oplus B_{n+1}$, and wherein G_n represents a Grey code bit n and B_n represents a binary code bit n.
27. A converter as in claim 25, wherein the drive code is obtained from the Grey code using the formula $D_k \,|_0^n = G_k \oplus G_{k+1} \oplus G_{k+2} \oplus \ldots \oplus G_n$, and wherein D_k represents a drive bit k.